Controllability of Novel $Sn_{0.95}Au_{0.05}$ Microbumps Using Interlaminated Tin and Gold Layers for Flip-Chip Interconnection

Kiyomitsu Onodera, Takao Ishii, Shinji Aoyama, and Masami Tokumitsu

***Abstract*—A flip-chip interconnection technology using novel lead-free solder microbumps with a balling temperature as low as 220 °C is presented. Controllability of newly developed $Sn_{0.95}Au_{0.05}$ microbumps has been examined experimentally. By varying the bump volume and the diameter of the wettable bump electrodes, $Sn_{0.95}Au_{0.05}$ microbumps with heights from 11 μm to 37 μm were successfully fabricated with a standard deviation of 1.5 μm. The deviation of on-chip CPW impedance from 50 Ω was lower than 10% for nonmetallization motherboard. The smaller bumps exhibited a better performance since the degradation of reflection properties is ascribed to the bump capacitance, which was estimated 10–20 fF. Because of high process yield and good performance, the flip-chip bonding using $Sn_{0.95}Au_{0.05}$ microbumps of the order of 20 μm in height may be advantageous for W-band interconnection of InP- or GaAs-based devices.**

I. Introduction

FLIP-CHIP interconnection using microbump bonding is one of the most promising approaches to meet the requirements for high-density packaging and high frequency performance [1], [2]. The advantages of solder bump bonding are low parasitic inductance and fine positioning and height accuracy due to the self-aligning nature of molten solder [3]. Lead-tin (Pb-Sn) solder is currently the most popular material because of low cost and wieldy properties. However, the increase awareness of lead's danger to the environment stimulated substantial research and development of lead-free solder. Although a lot of lead-free solders, including $Sn_{0.42}Bi_{0.58}$, $Sn_{0.48}In_{0.52}$, $Sn_{0.91}Zn_{0.9}$, *and* $Sn_{0.965}Ag_{0.035}$ are candidate for substitutes, these alloys cannot be made from the multi-layered films with a eutectic composition by sequential deposition. Because the constituent metals of these alloys do not exhibit interdiffusion and usually homogenized at 600 °C–800 °C. We have recently developed a novel lead-free microbump technique that uses interlaminated tin and gold layers for high-speed compound semiconductor ICs [4], [5]. Since the Sn-Au alloy system is a rare material which exhibits interdiffusion, the multiple layers can be homogenized at its eutectic temperature as low as 217 °C. This is low enough to apply to GaAs- or InP-based devices.

The bump design should be optimized to with the aim of ensuring low levels of reflection at the interconnection over a broad frequency range. The bump height and the bump bonding area may determine the variation in characteristic impedance and the parasitic capacitance of the interconnections. This letter reports an examination of the controllability of newly developed $Sn_{0.95}Au_{0.05}$ microbumps. The bump height could be accurately controlled by changing the bump volume and the diameter of the wettable bump electrodes. The relationship between the bump height and the performance of flip-chipped coplanar waveguide (CPW) has also been clarified.

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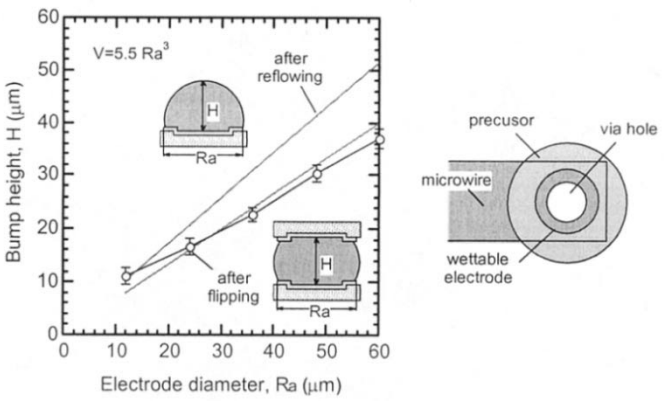


Fig. 1. Relationship between bump height, H, and diameter of bump electrode, R_a. Open circles are measured and broken lines are calculated. Relation between precursor diameter and bump volume was according to $V = 5.5R_a^3$.

II. Microbump Design and Fabrication

The geometry of the microbump, the bump electrode, and the microwire (CPW) is shown in Fig. 1. Microwires composed of Ti (100 nm)/Pt (500 nm)/Au (1500 nm) were fabricated on a GaAs wafer, laying 500 nm of SiO_2 underneath the microwire, and were coated with a 3.0 μm thickness of benzocyclobutene (BCB). The wettable bump electrodes, on which the microbumps would be laid, were composed of Ti (100 nm)/Pt (100 nm)/Au (100 nm). The bump electrodes and the microwires are connected through the via holes, which are 6 μm smaller in diameter than the bump electrodes. The bump electrode is shaped like a casserole with a rim. Precursors, which turn into bump balls after reflowing, were formed by a 15 μm-thick photoresist cavity. A multilayer film of tin and gold was sequentially deposited by electron beam evaporation. The total film thickness was 6.2 μm, and it was formed by ten cycles of sequential deposition, the thickness of each tin and

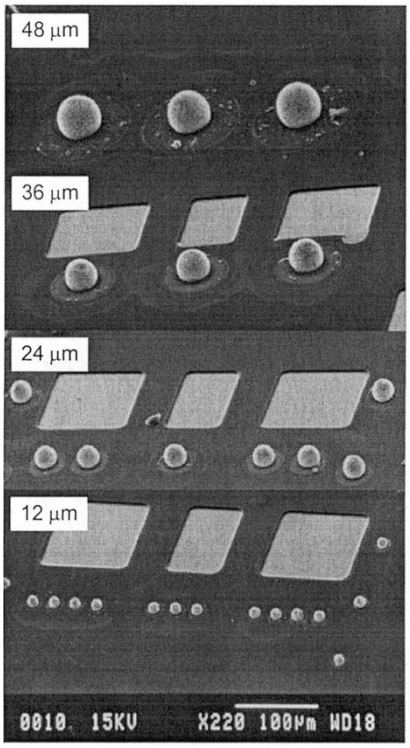


Fig. 2. SEM photographs of fabricated Sn-Au solder bumps after reflowing. Diameters of wettable metal terminals are 12, 24, 36, 48 μm.

gold layer being 600 nm and 20 nm respectively. After lift-off and resin flux coating, the precursors were heated to 220 °C for 2 min.

Fig. 2 shows SEM photographs of $Sn_{0.95}Au_{0.05}$ solder bumps after reflowing. The bump height could be precisely controlled by changing the bump volume and the diameter of the wettable bump electrode. The relation between diameter, R_a, and bump volume, V, was set as $V = 5.5R_a^3$.

The shape of a molten solder bump generally follows the Young-Laplace equation and is driven by the surface tension and the external pressure, i.e., the chip weight. The ratio of the chip weight to the surface tension, Mg/nTR_a, represents the influence of the chip weight on the bump shape, where Mg is chip weight, n is the number of bumps on the chip, and T is the surface tension.

Fig. 1 shows the bump height versus the diameter of the bump electrode. The broken line shows the calculated bump height on the assumption that the ratio $Mg/nTR_a \sim 0$. The open circles show the measured bump height after flip-chip connection. The GaAs chip weight is 12.7 mg, for the case where the chip size is 2 mm $\times$ 2 mm with a thickness of 0.6 mm. On each chip, bumps were laid on the chip periphery. The ratios Mg/nTR_a for each chip are in the range 0.23 to 0.43. The bump heights were estimated by measuring the gap of flip-chip samples using an infrared microscope. Measurements of 5 samples for each bump size were performed at the four corners of the chip. $Sn_{0.95}Au_{0.05}$ bump bonding with heights from 11 to 37 μm was successfully achieved with a high uniformity; standard deviations were as low as 1.5 μm. The measured bump height shows a gentler slope against diameter than that of calculated height because of the influence of the chip weight. Calculation indicates that the microbumps can be squashed by several percent in height in the case that $Mg/nTR_a \sim 0.3$. Then a new $Sn_{0.95}Au_{0.05}$ microbump can be designed and controlled as well as those using conventional $Sn_{0.6}Pb_{0.4}$. Meanwhile, the smallest bump seems to be taller than the calculated figure because the rim of the bump electrode is elevated on the 3-μm BCB.

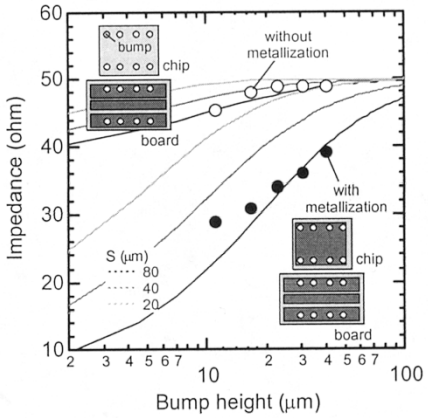


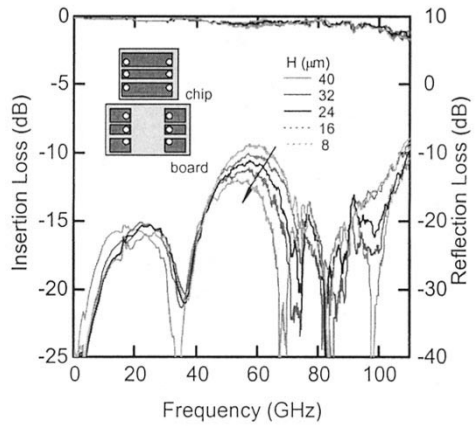
Fig. 3. Relationship of characteristic impedance and bump height. Plot was obtained by fitting measured S-parameters. Broken line is calculated by numerical simulation.

III. Measurement Results

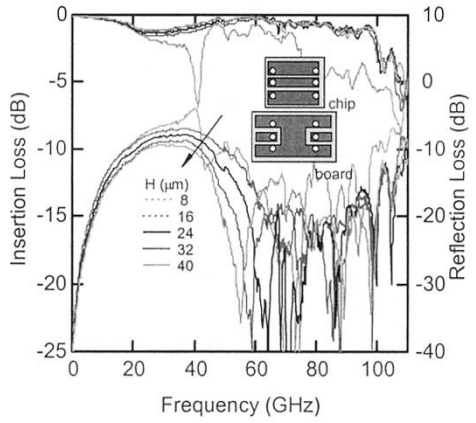
By means of flip-chip mounting, the circuit elements on the chip come close to the motherboard surface. As the microbump height is as low as just a few dozen microns, the presence of the motherboard might lower the impedance of the on-chip transmission lines. The bump height can also be evaluated by estimating the change in the characteristic impedance.

The 2.7-mm-long CPWs were fabricated on GaAs motherboards having many dummy bumps on the chip periphery to meet the condition that the ratio Mg/nTR_a is in the range from 0.23 to 0.43. GaAs chips with or without metallization on the surface were mounted face to face on the motherboards. The CPW width, S + 2W, was 200 μm, the slot width, W, 60 μm and the spacing, S, 80 μm. The relationship of characteristic impedance to measured bump height is shown in Fig. 3. The open and filled circles are measured results. The broken lines are calculated results by using conformal mapping. When the chip surface is not metallized, the deviation from 50 Ω is small and acceptable; it is only 10% even when the bump height is 11 μm. In case of metallization, a CPW could be regarded as CPW with a cover shield. The CPW impedance decreases drastically with decreasing bump height. The impedance is below 30 Ω when the bump height is less than 20 μm. The measured impedances agree well with the calculated ones. The filled circles lie above the calculated values for smaller bump sizes because of the influence of the SiO_2 underneath the microwires.

To evaluate the characteristics of the solder bump interconnections, GaAs chips and GaAs motherboards with CPWs were also fabricated. The width was 200 μm in both the chip and motherboard CPWs. The length of the chip CPW was 1.0 mm. After flip-chip mounting, the total length of CPW straddling the chip and motherboard became 2.7 mm. The solder bumps



(a)



(b)

Fig. 4. Measured reflection and insertion loss against frequency for flip-chip mounted CPWs. Motherboard surface beneath chip was (a) nonmetallized or (b) metallized.

were positioned at the end of the CPWs, where the centers of the bump electrodes were 20 μm inside the CPW edges. Two types of motherboard were also fabricated; the area underneath the flipped chip was metallized or nonmetallized as shown in the insets of Fig. 4. No impedance compensation was adopted on the bump-pad area so that nothing but the effect of bump bonding was evaluated.

Fig. 4 shows the measured reflection and insertion losses against frequency. In the nonmetallization case, the insertion loss is about 1 dB/mm at 110 GHz and is almost independent of the bump height. The bump height also has no significant influence on the reflection loss. The lower bumps, however, exhibit slightly better reflection at frequencies over 40 GHz. The reflection loss of 11-μm-height bumps is 5 dB better than that of 37-μm-height bumps. To reveal the bump capacitance, the measured S-parameters were fitted to the equivalent circuit. The CPW impedance in Fig. 3 was used and the bump bonding was modeled as a T-shaped circuit with shunt capacitance and series inductance. The bump parasitic capacitance was estimated to be 10 to 20 fF for bump heights from 11 to 37 μm, respectively. The higher the bump, the larger the bump capacitance. This is because a higher bump is equivalent to a fatter bump, due to the width-height aspect ratio being almost fixed for the solder bump, and a fatter bump results in a larger parasitic capacitance. The reflection properties are degraded more due to the bump parasitic capacitance than the mismatch of the impedance in the nonmetallization case.

When the motherboard is metallized, the reflection loss is much higher in the nonmetallization case. The higher the bump the better the performance, which is the same tendency as applies for the CPW impedance, as shown in Fig. 3. In the metallization case, the large reflection may be ascribed mainly to the mismatch of the CPW impedance. Moreover, the process yield of the bump bonding is considerably low in case of the smallest bumps, especially in metallized motherboard case. The resonance-like dip that occurred at around 40 GHz for a bump height of 11 μm, as shown in Fig. 4(b), may be due to a bad connection or a residue of flux. Because of high process yield and good performance, the flip-chip bonding using a bump height of the order of 20 μm and a motherboard without metallization may be advantageous for W-band interconnection.

IV. Summary

The controllability of newly developed $Sn_{0.95}Au_{0.05}$ microbumps manufactured from interlaminated tin and gold layers has been examined experimentally. By varying the bump electrode diameter and volume, $Sn_{0.95}Au_{0.05}$ microbumps with heights from 11 to 37 μm have been successfully fabricated. When the motherboard surface was not metallized, the deviation of CPW impedance from 50 Ω was small. Since the degradation of reflection properties may be ascribed to the bump capacitance, the smaller bumps exhibited a better performance. The bump parasitic capacitance was estimated to be 10 to 20 fF for bump heights from 11 to 37 μm respectively. New $Sn_{0.95}Au_{0.05}$ microbumps can be designed and controlled as well as those using conventional $Sn_{0.6}Pb_{0.4}$ and may be advantageous for W-band interconnection of high-speed compound semiconductor devices.

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